IN THE CLAIMS

Please cancel claim 1 and add the following claims:

1. (Canceled.)

2-24. (Previously Canceled.)

25. (New.) An integrated circuit master device comprising:

a first point-to-point link port to communicate with a buffer device of a first memory subsystem; and

a second point-to-point link port to communicate with a buffer device of a second memory subsystem.

26. (New.) The integrated circuit master device of claim 25, wherein the integrated circuit master device provides address, data, and control information to the first memory subsystem via the first point-to-point link port.

27. (New.) The integrated circuit master device of claim 25, wherein the integrated circuit master device receives data from the first memory subsystem via the first point-to-point link port.

28. (New.) The integrated circuit master device of claim 25 further including termination coupled to the first point-to-point link port.

29. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes:

transmitter circuitry to transmit data onto a first signal line; and

receiver circuitry to receive data from the first signal line.

30. (New.) The integrated circuit master device of claim 29, wherein data transmitted by the transmitter circuitry is multiplexed with data received by the receiver circuitry.

31. (New.) The integrated circuit master device of claim 29, wherein the transmitter circuitry transmits data and the receiver circuitry receives data simultaneously.

32. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port is configured to communicate using differential signaling.

33. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes unidirectional transmitter and receiver circuitry.

34. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes transmitter circuitry to output a differential data signal that includes encoded clock information.

35. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes receiver circuitry to receive a differential data signal that includes encoded clock information.

36. (New.) The integrated circuit master device of claim 25, further including an interface to communicate sideband signals to the buffer device of the first memory subsystem.

37. (New.) The integrated circuit master device of claim 36, wherein the sideband signals include reset instructions directed to at least one memory device included in the first memory subsystem.

38. (New.) The integrated circuit master device of claim 36, wherein the sideband signals include initialization instructions directed to at least one memory device included in the first memory subsystem.

39. (New.) The integrated circuit master device of claim 36, wherein the sideband signals include power management instructions directed to at least one memory device included in the first memory subsystem.

40. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes receiver circuitry to receive a multi-level pulse amplitude modulated signal.

41. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes transmitter circuitry to transmit a multi-level pulse amplitude modulated signal.

42. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes receiver circuitry to receive source-synchronous data from the first buffer device, wherein the source-synchronous data travels alongside a clock signal.

43. (New.) The integrated circuit master device of claim 25, wherein the first point-to-point link port includes transmitter circuitry to output a clock signal and source-synchronous data to the first buffer device, wherein the source-synchronous data is synchronous with respect to the clock signal and travels alongside the clock signal.

44. (New.) The integrated circuit master device of claim 25, wherein the integrated circuit master device is a processor device.

45. (New.) The integrated circuit master device of claim 25, wherein the integrated circuit master device is a controller device.

46. (New.) An integrated circuit device comprising:

a point-to-point link port to communicate data to a buffer device of a memory subsystem, the point-to-point link port including transmitter circuitry to output the data such that the data is synchronous with respect to a first clock signal and travels alongside the first clock signal; and

termination coupled to the point-to-point link port.

47. (New.) The integrated circuit device of claim 46, wherein the point-to-point link port includes receiver circuitry to receive data from the buffer device, wherein the data is

received synchronously with respect to a second clock signal and wherein the data travels alongside the second clock signal.

48. (New.) The integrated circuit device of claim 46, wherein the point-to-point link port is configured to communicate the data to the buffer device using differential signaling.

49. (New.) The integrated circuit device of claim 46, further including an interface to communicate sideband signals to the buffer device.

50. (New.) The integrated circuit device of claim 49, wherein the sideband signals include reset instructions to at least one memory device of the memory subsystem.

51. (New.) The integrated circuit device of claim 49, wherein the sideband signals include initialization instructions to at least one memory device of the memory subsystem.

52. (New.) The integrated circuit device of claim 49, wherein the sideband signals include power management instructions to memory devices of the memory subsystem.

53. (New.) An integrated circuit controller device comprising:

a first point-to-point link port to communicate data with a buffer device of a first memory subsystem, the first point-to-point link port including:

transmitter circuitry to output a first differential data signal that includes encoded clock information;

receiver circuitry to receive a second differential data signal that includes encoded clock information; and

termination coupled to the transmitter and receiver circuitry.

54. (New.) The integrated circuit controller device of claim 53, wherein the termination includes a first resistor coupled to the transmitter circuitry and a second resistor coupled to the receiver circuitry.

55. (New.) The integrated circuit controller device of claim 53, further including an interface to communicate sideband signals to the buffer device of the first memory subsystem.

56. (New.) The integrated circuit controller device of claim 55, wherein the sideband signals support reset instructions, initialization instructions, and power management instructions to memory devices of the first memory subsystem.

57. (New.) The integrated circuit controller device of claim 53, further including:

a second point-to-point link port to communicate data with a buffer device of a second memory subsystem; and

a third point-to-point link port to communicate data with a buffer device of a third memory subsystem.

58. (New.) An integrated circuit processor device that communicates data with a buffered memory subsystem via a point-to-point link, the integrated circuit processor device comprising:

transmitter circuitry to output data to the buffer device via a first external unidirectional signal line of the point-to-point link; and

receiver circuitry to receive data from the buffer device via a second external unidirectional signal line of the point-to-point link.

59. (New.) The integrated circuit processor device of claim 58, further including;

first termination coupled to the first external unidirectional signal line; and

second termination coupled to the second external unidirectional signal line.

60. (New.) The integrated circuit processor device of claim 58, further including an interface to communicate sideband signals that include reset instructions to the buffered memory subsystem.

61. (New.) The integrated circuit processor device of claim 58, further including an interface to communicate sideband signals that include initialization instructions to the buffered memory subsystem.

62. (New.) The integrated circuit processor device of claim 58, further including an interface to communicate sideband signals that include power management instructions to the buffered memory subsystem.

63. (New.) An integrated circuit processor device comprising a first point-to-point link port to communicate with a first buffered memory subsystem, wherein the first point-to-point link port comprises:

transmitter circuitry to transmit differential transmit signals to a first pair of external unidirectional point-to-point link endpoints, wherein the differential transmit signals are clocked synchronously with respect to a first clock signal, wherein the differential signals travel alongside the first clock signal;

receiver circuitry to receive differential receive signals from a second pair of external unidirectional point-to-point link endpoints, wherein the differential receive signals are clocked synchronously with respect to a second clock signal, wherein the differential signals travel alongside the second clock signal;

first termination coupled to the first pair of external unidirectional point-to-point link endpoints; and

second termination coupled to the second pair of unidirectional point-to-point link endpoints.

64. (New.) The integrated circuit processor device of claim 63, further including a second point-to-point link port to communicate with a second buffered memory subsystem and a third point-to-point link port to communicate with a third buffered memory subsystem.

65. (New.) The integrated circuit processor device of claim 63, further including an interface to communicate sideband signals that include reset instructions to the first buffered memory subsystem.

66. (New.) The integrated circuit processor device of claim 63, further including an interface to communicate sideband signals that include initialization instructions to the first buffered memory subsystem.

67. (New.) The integrated circuit processor device of claim 63, further including an interface to communicate sideband signals that include power management instructions to the first buffered memory subsystem.

68. (New.) An integrated circuit master device comprising:

a first point-to-point link interface means for communicating data with a buffer device of a first memory subsystem;

first termination means for terminating the first point-to-point link means;

a second point-to-point link interface means for communicating data with a buffer device of a second memory subsystem; and

second termination means for terminating the second point-to-point link means.

69. (New.) The integrated circuit master device of claim 68, wherein the first point-to-point link interface means includes:

transmitter means for transmitting data onto a first signal line; and

receiver means for receiving data from the first signal line.

70. (New.) The integrated circuit master device of claim 69, wherein the transmitter means and the receiver means are coupled to respective unidirectional signal lines of each of the first and second point-to-point links.

71. (New.) The integrated circuit master device of claim 68, wherein the first point-to-point link interface means includes:

transmitter means for transmitting a first differential data signal that includes first encoded clock information; and

receiver means for receiving a second differential data signal that includes second encoded clock information.